EXOSTIV IP

User Guide

Rev. 1.0.6 - February 13, 2024

Table of Contents

References

Revision History

Revision	Modifications
1.0.40	• Initial revision
1.0.3	• Screen shots update with latest software version
1.0.4	• General review with the launch of EXOSTIV Dashboard for Intel • Added references to RTL flow
1.0.5	• Legal and brand names update
1.0.6	• Updated figures • Updated FPGA devices and families. • Legal terms and names update. • Minor corrections,

EXOSTIV IP

Introduction

'EXOSTIV IP' is a configurable IP block that is configured and inserted into a target FPGA from EXOSTIV Dashboard. It aims at reaching and capturing the evolution over time of internal FPGA signals (FPGA 'nodes').

This user's guide provides information about EXOSTIV IP's structure, options and limitations. It describes how to configure and generate EXOSTIV IP from EXOSTIV Dashboard software.

In the two types of flow currently available, EXOSTIV Dashboard's Core Inserter is used to configure and synthesize EXOSTIV IP.

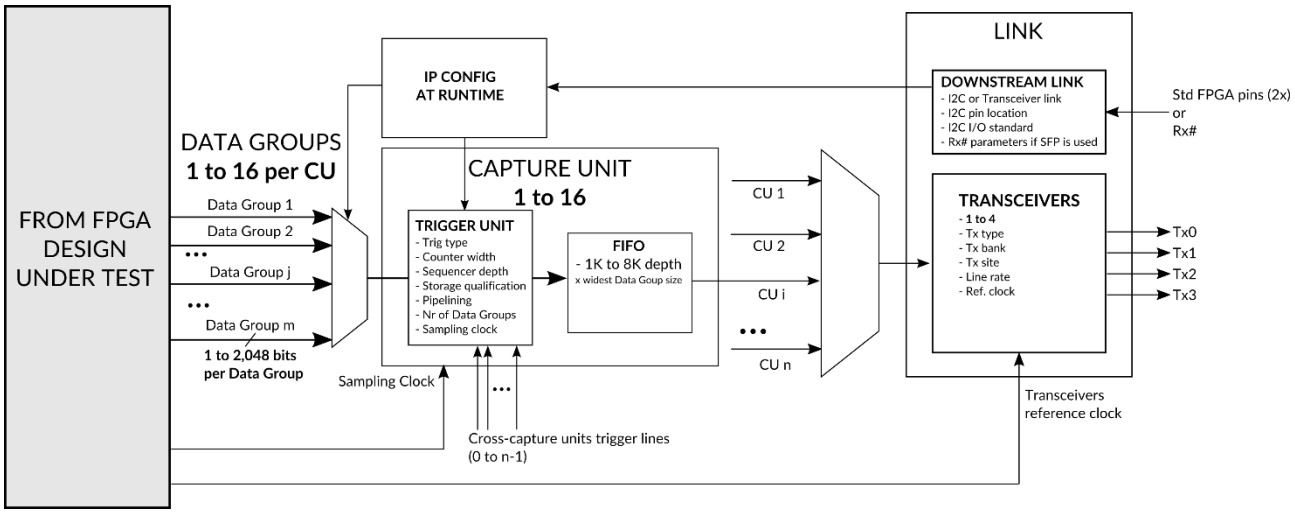
EXOSTIV IP is inserted into the target design either automatically at netlist level (after synthesis) if the **'netlist flow'** is used – or manually into the RTL code is the **'RTL flow'** is used.

The synthesis and/or the implementation (place & route) of the EXOSTIV IP and the (instrumented) target design is always performed with the FPGA vendor tools.

EXOSTIV IP is generated for diverse families of FPGA and programmable logic devices from AMD, Intel and Microchip.

Overview

Figure 1: EXOSTIV IP general view



Features

- Configurable upstream link, using 1 to 4 FPGA transceivers up to 12.5 Gbps[1]
- Downstream link to configure IP at run-time, without the need to re-implement instrumented design.
- From 1 to 16 configurable 'Capture Units' (CU) to sample FPGA internal nodes, with trigger and data qualification resources and selectable FIFO size.
- From 1 to 16 multiplexed Data Groups per CU, selectable at run time through downstream link.
- From 1 to 2,048 bits per Data Group, connected to the target FPGA internal nodes.
- Configurable clock signal for each capture unit, enabling multiple clock domains capture.
- Cross-CU trigger lines

[1] Target FPGA-dependent. The ability to capture at different speeds varies with the EXOSTIV Probe model.

Link Configuration

EXOSTIV IP LINK implements the connection with the EXOSTIV Probe. It is composed of 2 parts:

- The 'Transceivers' (or 'SERDES') that uses up to 4 FPGA transceivers. This resource is automatically shared by all the EXOSTIV IP's Capture Units – refer to section 'Capture Configuration'.
- The 'Downstream Link', that is used at runtime to change the IP settings at runtime (e.g.: the configuration of the multiplexers used to select the observed Data Groups).

EXOSTIV IP LINK is configured with the EXOSTIV Dashboard's Core Inserter.

Figure 2: EXOSTIV IP LINK configuration in EXOSTIV Dashboard

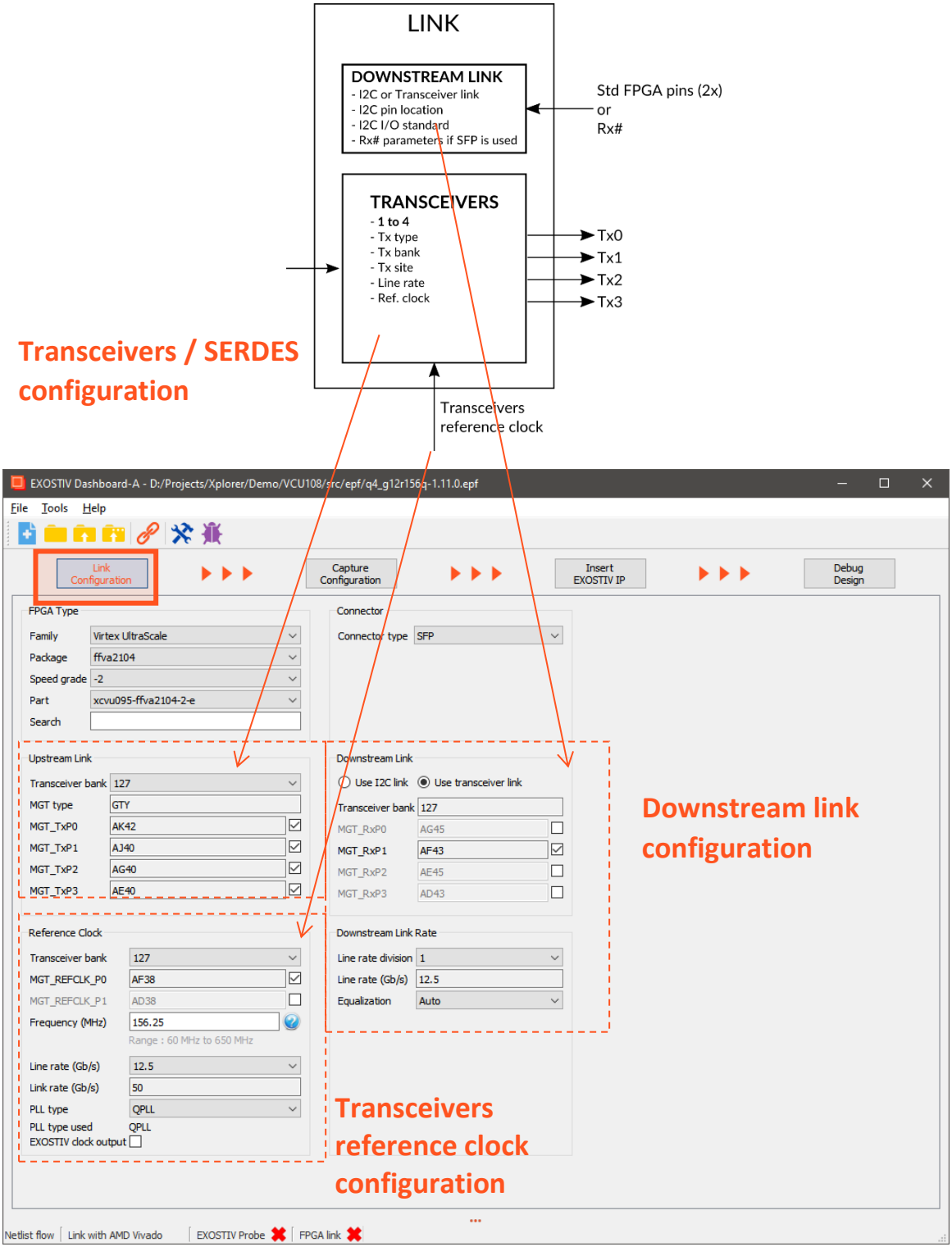


Table 1: FPGA Type parameters

Parameter	Description	Status and limitations
Family	Use dropdown box to select the target FPGA family.	**Supported families:** AMD, Intel and Microchip Click here for an updated list
Package	Use dropdown box to select the target FPGA package.	-
Speed grade	Use dropdown box to select the target FPGA speed grade.	-

Table 2: Upstream link parameters

Parameter	Description	Status and limitations
Transceiver bank	Use dropdown box to select the target FPGA bank of the transceivers used for EXOSTIV	**Check Note 'Upstream link implementation constraints' under this table.**
MGT Type	Informative, depends on the selected FPGA	
MGT_TxP0	Informative, shows the location of TxP0 in the selected transceiver bank. Select tick box to enable this transceiver with EXOSTIV.	
MGT_TxP1	Informative, shows the location of TxP1 in the selected transceiver bank. Select tick box to enable this transceiver with EXOSTIV.	
MGT_TxP2	Informative, shows the location of TxP2 in the selected transceiver bank. Select tick box to enable this transceiver with EXOSTIV.	
MGT_TxP3	Informative, shows the location of TxP3 in the selected transceiver bank. Select tick box to enable this transceiver with EXOSTIV.	

*Note: **Upstream link implementation constraints:***

1) *All transceiver channels must be in the same bank and: quad (AMD and Microchip) or 6-pack (Intel).*
2) *For each transceiver channel, the full differential pair (Tx and Rx) must be available. It is currently **not allowed** to share the transceiver channel resources (e.g. : Tx for EXOSTIV and Rx for another functionality).*
3) *For AMD devices, using the transceivers requires reserving a PLL resource from the channel. The requested line rate defines whether a CPLL can be used or if a QPLL must be used. The choice of the CPLL or the QPLL depends on the FPGA family, the chosen data rate and the frequency of the transceivers reference clock. This choice is made automatically by the EXOSTIV Dashboard interface when setting up the EXOSTIV IP link.*
4) *For Intel FPGA, EXOSTIV IP uses one fPLL from the 6-transceivers bank where the EXOSTIV is connected.*

Table 3: Reference Clock parameters

Parameter	Description	Status and limitations
Transceiver bank	Use dropdown box to select the transceiver bank from which the clock of the transceiver should be taken.	Refer to implementation constraints and DC & Switching characteristics of the target FPGA.
MGT_REFCLK_P0	Available reference clock selection. Use tick box to use this reference clock.	
MGT_REFCLK_P1	Available reference clock selection. Use tick box to use this reference clock.	
Frequency (MHz)	Use edit box or drop down list to specify the frequency of the transceivers reference clock picked from the FPGA under test.	
Line rate (Gb/s)	Use drop down list to select the transceivers' line rate in Gbit per second. The available choices are derived from the specified reference clock frequency.	
Link rate (Gb/s)	Informative: shows the total available bandwidth when using the selected transceivers at the specified line rate.	

Notes:

When reference clock frequency can be freely defined, (not a drop down), an utility used to evaluate the optimal frequency for a specific data rate can be opened from EXOSTIV Dashboard. Click on the '?' icon at the right of the Frequency (MHz) edit box () to open it.

In some software instances (e.g. Exostiv Dashboard for Microchip FPGA), the choice for the reference clock frequency is provided as a drop-down list. If you cannot find a suitable frequency in this list, please contact us and submit a formal request to extend the list of available frequencies.

Table 4: Connector parameters

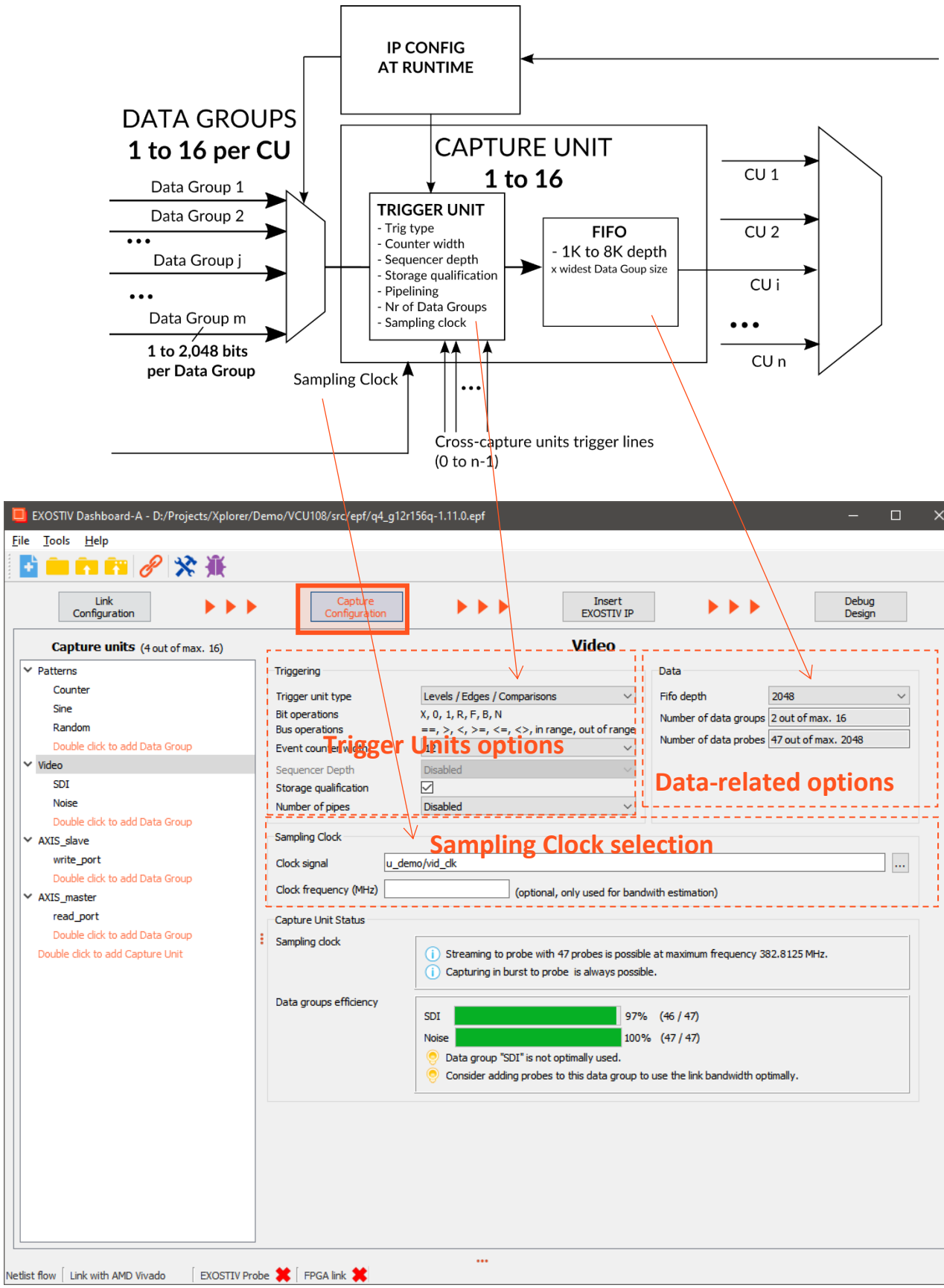
Parameter	Description	Status and limitations
Connector type	Use dropdown list to select the physical connection on EXOSTIV Probe, HDMI or SFP. ***The HDMI type of connector with I2C side band for control is scheduled to be phased out in future versions of the Exostiv probe. It is therefore not recommended for new designs.***	When HDMI is selected, only the I2C link that uses FPGA standard pins is available. When SFP is selected, the downstream link uses one of the transceivers Rx.

Table 5: Downstream Link parameters

Parameter	Description	Status and limitations
Link type selection radio buttons	Use radio button to select: **I2C link:** this option requires using 2 extra pins on the FPGA package for the downstream link **Use transceiver link:** this option implements the downstream link with one the transceivers Rx.	When HDMI is selected, only the I2C link that uses FPGA standard pins is available. When SFP is selected, the downstream link uses one of the transceivers Rx.
Downstream Link parameters if I2C link is selected		
SCL package pin	Specifies the target FPGA pin on which the SCL signal of the downstream link is connected.	
SDA package pin	Specifies the target FPGA pin on which the SDA signal of the downstream link is connected.	
SCL I/O standard	Use dropdown box to select the I/O standard for SCL	
SCL I/O standard	Use dropdown box to select the I/O standard for SDA	
Downstream Link parameters if 'Use transceiver link' is selected		
Transceiver bank	Specifies the transceiver bank in which the downstream link is implemented.	
MGT_RxP0	Informative, shows the RxP0 pin location in the selected bank of the selected FPGA. Select the tick box to use it for the downstream link.	Only one of the transceivers has to be selected for the downstream link.
MGT_RxP1	Informative, shows the RxP1 pin location in the selected bank of the selected FPGA. Select the tick box to use it for the downstream link.	
MGT_RxP2	Informative, shows the RxP2 pin location in the selected bank of the selected FPGA. Select the tick box to use it for the downstream link.	
MGT_RxP3	Informative, shows the RxP3 pin location in the selected bank of the selected FPGA. Select the tick box to use it for the downstream link.	

Capture Configuration

Figure 3: EXOSTIV IP Capture configuration in EXOSTIV Dashboard



The ‘Capture Configuration’ window is used to define the Capture Units and their characteristics.
The window’s contents changes according to the context. It is divided in 2 main panes:

- A column on the left side of the window provides an overview of the defined Capture Unites and their data groups.
- The main content window changes when a specific capture unit or a related data group is selected from the left side column.

Figure 3 shows the contents of the window when a Capture Unit (‘Capture Unit 1’) is selected. **Figure 4** shows the contents of the window when a data group (‘Sine’ data group of ‘Capture Unit 1’) is selected.

Figure 4: EXOSTIV IP Capture configuration in EXOSTIV Dashboard – Data group options *(netlist flow only)*

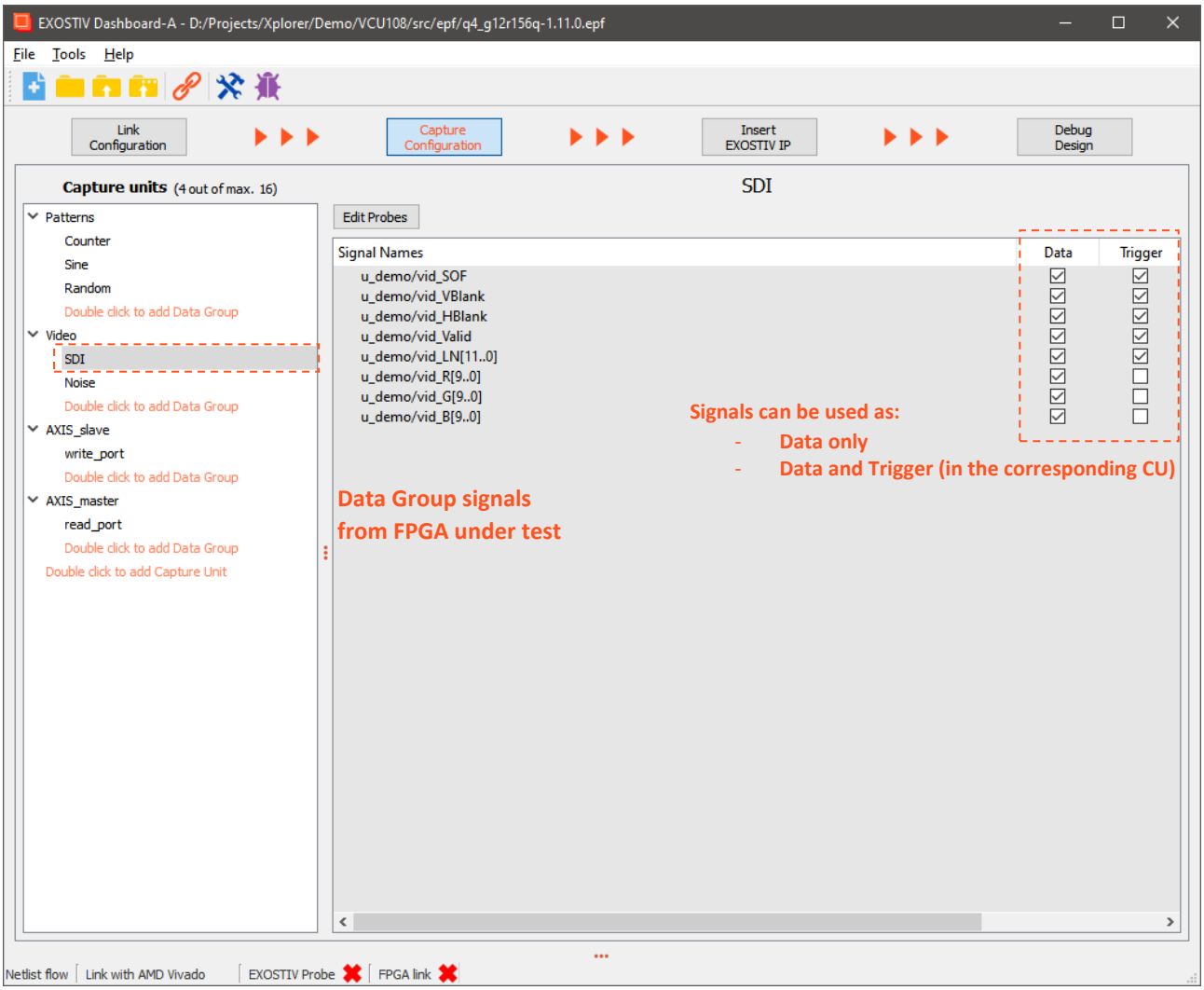


Table 6: Triggering parameters (refer to Figure 3)

Parameter	Description	Status and limitations
Trigger unit type	Use dropdown box to select between: 'Levels / Edges / Comparisons' 'Level /Edges'	Disabling comparisons saves on the logic needed to implement the capture units but does not allow triggering capture on inequalities or value ranges for bus operations.
Bit operations	Informative: shows the types of arguments that can be used for the triggering conditions at bit level. X : don't care 0 : logic 0 1 : logic 1 R : Rising edge F : Falling edge B : Both edges N : No edge / No transition	
Bus operations	Informative: shows the types of arguments that can be used for the triggering conditions at bit level. == : equality > : greater than < : smaller than >= : greater than or equal to <= : smaller than or equal to in range : trigger when inside the specified value range out of range : trigger when outside the specified value range	
Counter width	Use dropdown box to specify the width in number of bits of an event counter for the trigger. Legal values: Disabled, or 1 to 32 bits.	
Sequencer depth	Use dropdown box to implement a sequencer and specify the number of stages needed. This sequencer is used to implement sequential trigger conditions.	Not available in current Dashboard version. Please contact us for roadmap and availability.
Storage qualification	Select tick box to enable 'storage qualification conditions' at runtime. Storage qualification enables filtering captured data according to a logic condition defined on it (e.g., only capture data if a 'data enable' signal is active).	
Number of pipes	Use drop down box to enable and insert pipelining in the data path of this capture unit. Up to 8 stages can be added for each data group before the data group selection multiplexer.	

Table 7: Data parameters (refer to Figure 3)

Parameter	Description	Status and limitations
Fifo[1] Depth	Use dropdown to select the Capture Unit's Fifo depth. Values can be chosen between 1,024 – 2,048 – 4,096 – 8,192	The Fifo is used as a temporary buffer to accommodate for different clock rates at the input of EXOSTIV IP and at the transceivers level. The Fifo size also defines the maximum burst size in 'Burst Mode' when capturing data.
Number of data groups	Use dropdown box to specify the desired number of data groups for the selected capture unit. 1 to 16 data groups can be defined.	Using more than one data groups inserts a multiplexer at the input of the capture unit. This multiplexer can be switched at runtime to enable observation of a reduced set of data and save on the transceivers' bandwidth.
Number of data probes	Informative: shows the width of the data bus used for the capture unit, according to the chosen data groups and the connected nodes.	

[1] *The Fifo width is automatically selected as the size of the widest of the connected Data Groups.*

Table 8: Sampling Clock (refer to Figure 3) ***(netlist flow only)***

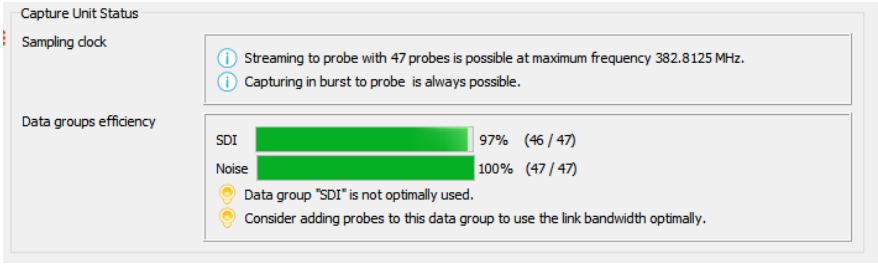
Parameter	Description
Clock signal	This this edit box to specify the clock signal from the FPGA design under test, that has to be used as a sampling clock for the specified connected nodes. Click on the '…' button to open a dialog and select the clock signal from the loaded target design (refer to **Figure 5**).
Clock Frequency (MHz)	In this field, the sampling clock frequency for the chosen capture unit can be specified in MHz. This features allow computing the 'Capture unit Status', and evaluate whether streaming can be achieved with the specified CU sampling clock. Please refer to Exostiv Dashboard user's guide or Exostiv Labs knowledge base for more details about this feature. 

Table 9: Data groups parameters (refer to Figure 4)

Description
The main window shows the list of the FPGA nodes selected for the active Data Group. Select the 'Data' and 'Trigger' tick box to enable using the corresponding nodes as 'data only' or as 'data AND trigger'. If a signal is selected as a 'trigger', a trigger condition can be defined on it at runtime to capture data. In **netlist flow only,** clicking on the **'Edit Probes'** button opens a dialog box to select the list of signals from the loaded target design (refer to Exostiv Dashboard user's guide). In **RTL flow,** it is not allowed to connect the probes from the Dashboard interface, as this has to be done 'manually' by the user at RTL level. The 'connections' are simply the result of instantiating and connecting EXOSTIV IP from inside the RTL code.

Figure 5: Capture Unit sampling clock selection dialog box

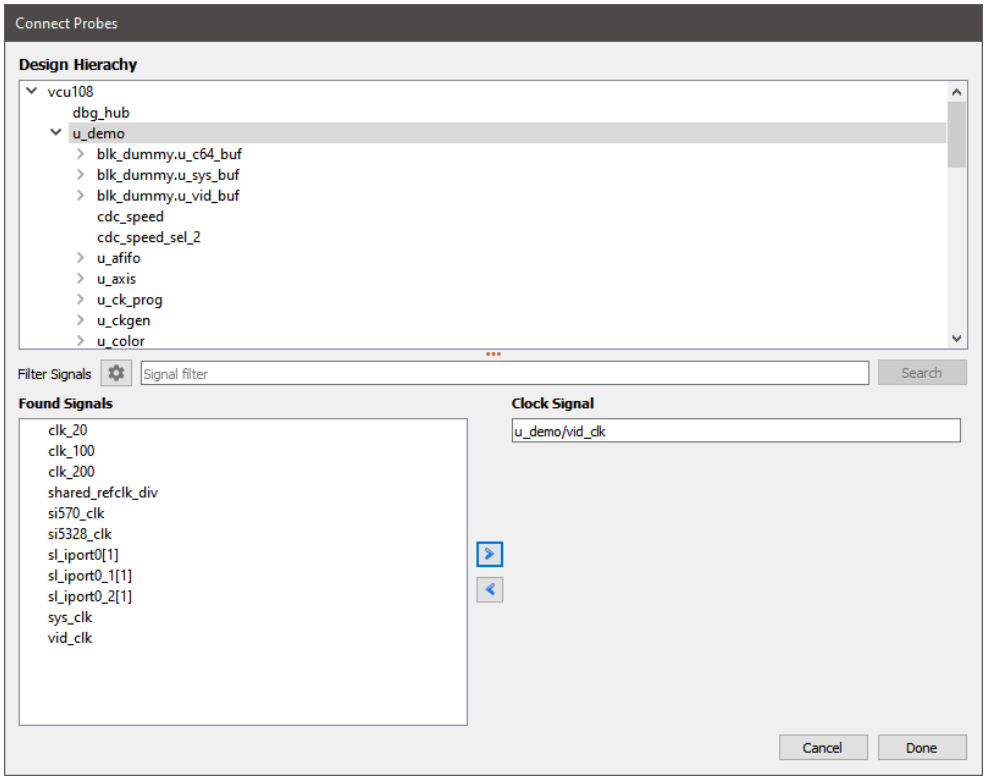
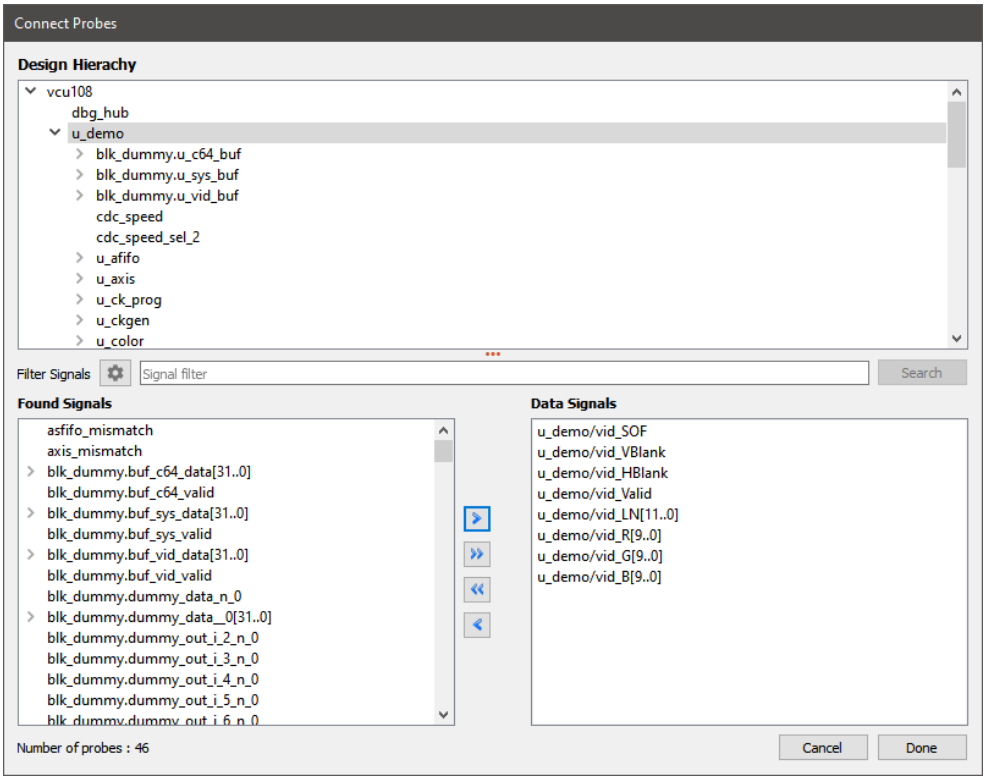


Figure 6: Capture Unit probes connection dialog box



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